BMS COLLEGE OF ENGINEERING, BENGALURU-19
Autonomous Institute, Affiliated to VTU
Department of Electronics and Communication Engineering

Scheme and Syllabus
M. Tech (VLSI Design and Embedded systems)
Batch 2020 onwards

INSTITUTE VISION

Promoting Prosperity of mankind by augmenting human resource capital through Quality Technical Education & Training

INSTITUTE MISSION

Accomplish excellence in the field of Technical Education through Education, Research and Service needs of society

DEPARTMENT VISION

To emerge as a Centre of Academic Excellence in Electronics, Communication and related domains through Knowledge acquisition, Knowledge dissemination and knowledge generation meeting global needs and standards.

DEPARTMENT MISSION

***Imparting quality education through state of the art curriculum, conducive learning environment and Research with scope for continuous* improvement *leading to overall Professional Success*.**

PROGRAM EDUCATIONAL OBJECTIVES

The department has defined the following PEOs for the PG programme in VLSI Design & Embedded system.

PEO-1:

Graduates shall be capable of building their career in industries, R&D establishments as well as in academia in the domain of VLSI Design and Embedded systems.

PEO-2:

Graduates shall be capable of conducting research leading to technology solutions of societal importance.

PEO-3:

Graduates shall collaborate, manage and execute projects in teams using relevant tools/technologies and demonstrate professional behavior.

PROGRAM OUTCOMES

Program Outcomes (POs), are attributes acquired by the student at the time of graduation. These attributes are measured at the time of Graduation, and hence computed every year for the outgoing Batch. The POs are addressed and attained through the Course Outcomes (COs) of various courses of the curriculum.

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

Distribution of credits

Category	No of Credits
Program Core Course	26
Program Elective Course	15
All programme core Course	02
Open Elective Course	04
Internship	9
Technical Seminar	04
Audit Courses	4 Units
Project Work	28

Total Number of Credits (I Sem – IV Sem) = 88 Credits

Distribution of Marks

For each subject CIE will be conducted for 50, SEE for 100 (will be reduced to 50) and hence total marks of 100 are allotted to each subject including CIE(50) and SEE (50)

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I Semester **CREDIT BASED**

Subject Code	Course Title	CREDITS			
		L	T	P	
20ECVEBSAM	Applied Mathematics	3	0	0	3
20ECVEPCDI	Digital IC design	3	0	1	4
20ECVEPCES	Embedded Software and Hardware Architecture	3	0	1	4
20ECVEPCAI	Analog IC design	3	0	0	3
20ECVEPEZZ	Elective -1	3	0	0	3
20ECVEPEZZ	Elective -2	3	0	0	3
20ALLPICRM	Research Methodology & IPR	2	0	0	2
Total		20	0	2	22

Note: Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

Elective -1 and Elective -2			
20ECVEPEST	Static Timing Analysis	20ECVEPELP	Low Power VLSI Design
20ECVEPECA	Advanced Computer Architecture	20ECVEPEEC	Embedded Computing and Networking
20ECVEPEMP	Device Modelling and Processing Technology	20ECVEPEAV	Advances in VLSI Structure

Note: (i) The Course Code Expansion: Ex.: 18ECVEBSAM: 20 = Year of syllabus introduced / revised, EC = Dept., VE = Program, BS = Basic Science, AM = Advanced Mathematics.

PC/PE: Program Core / Program Elective, GC/GE: Group Core / Group Elective, OE: Open Elective.

ZZ (course abbreviation of Electives),

(ii) Exception for 18ALLPICRM: ALLP = All Program, I = Institution C = Core, RM = Research Methodology.

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II Semester **CREDIT BASED**

Subject Code	Course Title	CREDITS			
		L	T	P	
20ECVEPCMS	Mixed Signal Circuit Design	3	0	1	4
20ECVEPCDT	Design for Testability	3	1	0	4
20ECVEPCRT	Real Time Operating Systems	3	0	1	4
20ECVEPEZZ	Elective -3	3	0	0	3
20ECVEPEZZ	Elective -4	3	0	0	3
20ECVEOEZZ	Open Elective	4	0	0	4
Total		19	1	2	22

Note: Two electives to be chosen from the list below:
Elective will be offered for a minimum strength of six candidates (out of 18) / eight candidates (out of 24)

Elective -3 and Elective -4			
20ECVEPESV	System Verilog and verification	20ECVEPEPD	Physical Design
20ECVEPEHS	Hardware-Software Co-design	20ECVEPEMD	Memory Design and Testing
20ECVEPESC	System On Chip Architecture	20ECVEPEDS	Digital System Design Using FPGAs

Open Elective

20ECVEOESL	Introduction to scripting languages

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III Semester **CREDIT BASED**

Subject Code	Course Title	CREDITS			
		L	**T**	**P**	Total
20ECVEGEZZ	Elective 5	2	1	0	3
20ECVEPWP1	Project Work-Phase-1	0	0	8	8
20ECVEPCIN	Internship	0	0	9	9
20ECVESR01	Technical Seminar-1	0	0	2	2
20ECVENCA1	Audit course -1	0	0	0	2 units
Total		2	1	19	22

Elective 5			
20ECVEPEAD	Advanced Digital System Design Using FPGAs	20ECVEGEML/ 20ECELGEML	Machine Learning and AI
20ECVEGEUV/ 20ECELGEUV	UVM Methodology concepts		

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IV Semester **CREDIT BASED**

Subject Code	Course Title	CREDITS			
		L	**T**	**P**	Total
20ECVESR02	Technical Seminar-2	0	0	2	2
20ECVEPWP2	Project Work-Phase-2	0	0	20	20
20ECVENCA2	Audit Course-2	0	0	0	2 units
Total		0	0	22	22

Course Title	APPLIED MATHEMATICS				
Course Code	20ECVEBSAM	Credits	3	L-T-P	3:0:0
CIE	50 Marks(100% weightage)	SEE		100 Marks (50% weightage)	

At the end of this course, student will have the ability to:

CO	Course Outcomes	PO
CO1	Demonstrate knowledge and understanding of the underlying concepts of random variables and stochastic processes	PO3
CO2	Demonstrate knowledge of the mathematical concepts and computational aspects of linear algebra and graph theory	PO3
CO3	Analyse domain related engineering problems and develop analytical problem solving approach making use of the theoretical concepts	PO3

Unit- I **08 hrs**

Review of basic probability theory. Definition of random variables and probability distributions, probability mass and density functions, expectation operator, illustrative examples

Unit- II **07 hrs**

Moments, central moments, characteristic functions, probability generating functions - illustrations Poisson, Gaussian and Erlang distribution examples. Pair of random variables – Joint PMF, PDF, CDF.

Unit- III **06 hrs**

Random Processes - Classification. Stationary, WSS and ergodic random process. Auto-correlation function-properties, Gaussian random process, Engineering Applications of Random processes.

Unit- IV **08 hrs**

Linear Algebra: Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear

transformations-definitions, Matrix form of linear transformations - Illustrative examples, Computation of Eigen values and Eigen vectors of real symmetric matrices - Given's method.

Unit- V **07 hrs**

Computational Graph Theory: Graph enumerations and optimization: DFS-BFS algorithm, shortest path algorithm, min-spanning tree and max-spanning tree algorithm, basics of minimum cost spanning trees, optimal routing trees, optimal communication trees, network flow algorithms

Text Books:

1. S L Miller and D C Childers**, "Probability and random processes: application to signal processing and communication**", Academic Press / Elsevier 2004.

2. David C. Lay, "**Linear Algebra and its Applications**", 3rd Edition, Pearson Education, 2003.

3. GeirAgnarsson and Raymond Greenlaw "**Graph Theory- Modeling, Applications and Algortihms",** Pearson Education, 2007.

Reference books:

1 A. Papoulis and S U Pillai, **"Probability, Random variables and stochastic processes",** McGraw Hill 2002

2 Roy D. Yates and David J. Goodman, **Probability and Stochastic Processes: A friendly introduction for Electrical & Computer Engineers**/

3. MIT Open courseware**, Introduction to Linear Algebra, Course 20.06**

4 NausingDeo, "**Graph Theory with applications to Engineering and Computer Science**", Prentice Hall of India, 1999.

Course Title	**DIGITAL IC DESIGN**				
Course Code	**20ECVEPCDI**	**Credits**	**4**	**L-T-P**	**3:0:1**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisite:

The Metal Oxide Semiconductor (MOS) Structure, Network theory, Fundamentals of HDL.

Course outcomes:

At the end of the course, the student will have the ability to:

CO	**Course Outcomes**	**PO**

CO1	Analyse the given circuit to arrive at the specification	**PO3**
CO2	Design**,** write program and simulate Static and Dynamic circuits to meet the specification	**PO3**
CO3	Engage in literature survey in a group on the topic related to course and submit a detailed report	**PO2**

Unit- I **08 hrs**

MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, Static Characteristics of MOS Inverters: Resistive load inverters, CMOS Inverter.

Unit- II **08 hrs**

MOSFET Scaling and Small-Geometry Effects,

Structure and operation of SOI MOSFETS, Double gate to Multi gate MOSFET, Carbon nanotubes. BSIMCMG, a compact model for multi gate transistors.

Unit- III

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

Unit- IV **07 hrs**

Circuit Simulation: Sources and Passive Components, Transistor DC Analysis, Inverter Transient analyses, Sub circuits and measurements, Optimization**,** SPICE Commands, Level 1 model, Level 2 and 3 models, BSIM Models, Design Corners. Other SPICE commands.

Unit- V **08 hrs**

Principles of RTL Design: Verilog Coding Concepts, Verilog coding guide lines: Combinational, Sequential, FSM. General Guidelines, Synthesizable Verilog Constructs, Sensitivity List, Verilog Events, RTL Design Challenges.

Text Books

1. Sung Mo Kang &YosufLeblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition.

3. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition

Reference Books

4. Verilog HDL Synthesis A Practical Primer by J. Bhasker

5. Fundamentals of Digital Circuits by A. Anand Kumar, 2nd Edition

6. Principles of VLSI RTL Design: A Practical Guide by Sanjay Churiwala ,SapanGarg, 2011

7. FinFETs and Other Multi-Gate Transistors by J.-P. Colinge springer.com

MOOCs:

1. https://swayam.gov.in/nd1_noc20_ee05/preview
2. https://nptel.ac.in/courses/108/106/108106158/
3. https://www.youtube.com/watch?v=IXjNLK7GC70&list=PL3pGy4HtqwD15wr99U4CBhYqiZIwWbl12

LABORATORY EXPERIMENT LIST

Sl.No	Title of the Experiments
	PART-1
1.	Design inverter circuit schematic and layout for the given specification (Noise Margin, Power, delay etc.), given technology (CMOS, FINFET, SOI etc.) by using EDA tools.
2.	Design NAND Gate schematic and layout for the given specification (Noise Margin, Power, delay etc.) given technology (CMOS, FINFET, SOI etc.)by using EDA tools.
3.	Design SRAM circuit schematic and layout for the given specification (Noise Margin, Power, delay etc.) given technology (CMOS, FINFET, SOI etc.)by using EDA tools.
4.	Design Dynamic circuits, for the given specification (Noise Margin, Power, delay etc.) given technology (CMOS, FINFET, SOI etc.)by using EDA tools.
	PART-2
1.	Use V_{DD}=1.8V for 0.20um CMOS process, V_{DD}=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
1.a	**Input Characteristics Analysis** a) Plot and analyse I_D vs. V_{GS} at different drain voltages for NMOS, PMOS. Determine V_t b) Plot log I_D vs. V_{GS} at particular gate voltage (high) for NMOS, PMOS and determine I_{OFF} and sub-threshold slope.

1.b	**Output Characteristics Analysis** a) Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel Length modulation factor. b) Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, plot DC load line and calculate g_m, g_{ds}, g_m/g_{ds}, and Unit-y gain frequency. Tabulate your result according to technologies and comment on it.
2.	Use V_{DD}=1.8V for 0.20um CMOS process, V_{DD}=1.2V for 0.13um CMOS Process and V_{DD}=1V for 0.09um CMOS Process.
2.a	Perform the following i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in} and determine Transition voltage. Calculate V_{IL}, V_{IH}, N_{MH}, N_{ML} for the inverter. ii. Plot VTC for CMOS inverter with varying V_{DD}. iii. Plot VTC for CMOS inverter with varying device ratio.
2.b	Perform transient analysis of CMOS inverter with no load and with load and determine t_{pHL}, t_{pLH}, 20%-to-80% tr and 80%-to-20% tf. (use V_{PULSE} = 2V, C_{load} = 50fF)
2.c	Perform AC analysis of CMOS inverter with fan-out 0 and fan-out 1. (Use C_{in}= 0.012pF, C_{load} = 4 PF, R_{load} = k)
	PART-3
3.	Design, Write Verilog code for the circuits for the given specification, Simulate, and synthesize, view report, Use EDA Tools like Cadence, Mentor Graphics, and Synopsis. 1. FSM 2. Memory

Course Title	**Embedded Software and Hardware Architecture**				
Course Code	**20ECVEPCES**	**Credits**	**4**	**L-T-P**	**3:0:1**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisites:

Introductory course on Embedded Systems, Microcontrollers (any), Basic C Programming Skills

Course outcomes:
At the end of the course, the student will have the ability to:

CO	Course Outcomes	PO
CO1	Analyze the advanced features of ARM processors to develop efficient Embedded Systems	PO3
CO2	Develop and analyze the performance of C programs for execution on microcontroller/SOC development board based on ARM architecture. Develop Python programs to interface with Embedded Systems.	PO3
CO3	Develop embedded systems using different approaches	PO3
CO4	Engage on market survey of various available embedded hardware and software architecture for performance, power and cost optimization. Present a report on the same.	PO1,2

Unit--I **10 hrs**

ARM architecture: ARM product profiles and features, Cortex M features and applications, performance, operation modes and privilege levels, switching of operation modes, register classification and importance, memory map, advantages of bit band region, aligned and unaligned access, endianess and performance, SYSTICK timer and interrupt, exception types, NVIC, interrupt and execution sequences, vector fetches, tail chaining, faults caused by exceptions, ARM busses and their role to enhance performance.

Unit--II **10 hrs**

Embedded C Programming: C and embedded C data types, bit manipulation,advanced pointer use, function pointers arrays and dynamic memory allocation, introduction to data structures, enumerations, unions, structures and encapsulation, bit fields, LIFO buffer, circular buffer, linked list. Modular C programming, writing header files and exception handlers.
ARM memory access using variables and pointers, design of CPU Core and Peripheral register structures using bit fields, IO port configuration example, creating software interfaces for hardware, Pre-processor directives in C. Storage Classes of C. Storage type qualifiers, inline assembly, performance optimization through appropriate data type selection and data alignment.

Unit--III **08 hrs**

Python Programming: Introduction Python Programming, data types, lists, tuples, dictionaries, conditional statements, iterative statements, functions. File and I/O handling, serial device interfaced to external devices. Strings and data formatting, integer, bytes, hexadecimal representation, embedded programming using python case studies, UI design (arduino/RPi).

Unit--IV **05 hrs**

Firmware Architecture for Embedded Systems: Super Loop, Interrupt driven, RTOS, CMSIS RTOS, Low Power Operations. Speed Power Product, Optimization for time and space.

Unit--V **06 hrs**

Develop an embedded system using different approaches: using GPP, using FPGA and as a SPP. Debugging Techniques for Embedded Systems: Introduction to GNU Debugger gdb. uVision IDE based debugging techniques. Single Stepping, Break Points, Watch Points, and Memory Probing. Simulation using uVision.

Text Books:

1. Joseph Yiu, "Definitive guide to the ARM Cortex-M3", Latest available edition
2. Hennessy and Patterson, "Computer Architecture: A Quantitative Approach", Latest available edition
3. Michael J Pont, "Embedded C", latest available edition
4. Leonard Edison, "Python Programming", latest available edition

Reference Books:

1. Technical reference manual and datasheets of Cortex-M3 microcontroller and other components.
2. Shibu K V, "Introduction to Embedded Systems", Latest available edition
3. And many other online tutorials and references.

E Books:

1. Joseph Yiu, "Definitive guide to the ARM Cortex-M3", Latest available edition
2. Practical C Programming, 3rd Edition by by Steve Oualline, Publisher(s): O'Reilly Media, Inc. ISBN: 9781565923065
3. Introducing Python, 2nd Edition by Bill Lubanovic Released November 2019 Publisher(s): O'Reilly Media, Inc. ISBN: 9781492051367

MOOC/Online courses:

- Embedded Software and Hardware Architecture by University of Colorado Boulder – Coursera
- Embedded system Design IIT by AnupamBasu, IIT Kharagpur https://nptel.ac.in/courses/106/105/106105159/

LABORATORY EXPERIMENT LIST

Sl.No	Title of the Experiments
	PART 1
1.	Install Keil MDK for ARM along with development board drivers. Interface development board to development PC. Download and test blinky code example.
2.	Develop a super loop to transmit ADC data on UART every 'x' Unit-s of time.
3.	Receive data from an analog sensor, digitize it and send it to display Unit-.
4.	Develop an interrupt routine to accept 100 bytes of data from sensors and send out on SPI or I2C bus. Consider buffering and non-buffering approaches.
5.	Develop an interrupt routine to control any actuator aa per given specifications.
6.	Configure port pin to function as external interrupt and develop interrupt handler as per specifications (discussed in class).
	PART 2

1.	Develop services and instantiate them in different ways.
2.	Create structures to realize special registers of ARM microcontroller.
3.	Develop APIs to access individual bits/nibble/whole register contents and to configure MC for specific modes.
4.	Create APIs to realise exception facilities as in ARM controllers (use unions).
	PART 3
1.	Create databases using python scripts. Store sensor data as a database.
2.	Develop Python code to interface external peripherals.
3.	Create webpages using python scripts.
4.	Read data from webpage using python program and transfer the same to microcontroller over UART.
5.	Post data on to any webpage using Python.
6.	Send emails using Python program.
7.	Receive data from microcontroller on to PC using Python and either email that data or post it on to any webpage.

NOTE: Any ARM Cortex M development board can be used. Audrino/RPi can be used to port python codes.
Platform used: Kiel uVision MDK IDE, C compiler on Windows. Lab and Theory sessions are integrated.

Course Title	**ANALOG IC DESIGN**				
Course Code	**20ECVEPCAI**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisite:

Analog Integrated circuit, Linear IC Design

Course outcomes:

At the end of the course, the student will have the ability to:

CO	**Course Outcomes**	**PO**
CO1	Develop methods for quantifying the Analog circuits by inspection, aiming Analog design octagon**.**	**PO3**
CO2	Design stable Analog Integrated Circuits to meet given specification	**PO3**

CO3	Demonstrate Different Operational amplifier topologies through literature survey in groups.	**PO1,2**

Unit-I **08 hrs**

MOS I/V Characteristics, second order effects, MOS device models. Basics of single stage amplifiers

Unit-II **08 hrs**

Design and Analysis of Gain, Input, output Impedance of single stage amplifiers, frequency response of Common-Source and Source Follower

Unit-III **08 hrs**

Differential Amplifiers: Design and analysis of Differential Amplifiers for a given specification.

Unit-IV **08 hrs**

Current Mirrors current mirrors, Cascade mirrors and active current mirrors

Noise: Types of noise, Noise in Single stage amplifier.

Unit-V **07 hrs**

Design of Two Stage Operational amplifier, Folded Cascode Operational amplifier, Telescopic operational amplifier

Text Books:

1. "Design of Analog CMOS Integrated Circuits", Behzad Razavi, TMH, 2007.

2. Paul. R.Gray, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, (4/e), 2001

Reference Books:

1. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Second Edition, Wiley.
2. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition, Oxford University Press.

MOOCs:

1. https://nptel.ac.in/courses/117/106/117106030/
2. https://www.youtube.com/watch?v=311XkpNGs8c

I Semester electives

Course Title	**STATIC TIMING ANALYSIS**				
Course Code	**20ECVEPEST**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisites:

Courses on Digital circuit design, knowledge about combinational circuits, synchronous and asynchronous circuits. Courses on Semiconductor devices characteristics

Course outcomes:

At the end of the course, the student will have the ability to

CO	Course Outcomes	PO
CO1	**Apply** the learnt basic concepts of STA to evaluate the delay of the circuits and **analyse** the generated report to identify critical issues and bottleneck for the violation and **suggest** the techniques to make the design to meet timing	PO3
CO2	**Write** their own constraint file and create the environment required for the given design and its specification to undergo for **analysis using the EDA tool.**	PO2,3
CO3	Understand the **journal research papers related to Timing analysis techniques** and able to present suitable techniques for the given design.	PO1,3

Unit-I **08 hrs**

Introduction: Basics of timing concepts

Delay Concepts for Digital Designing: Types of Delays in Digital Circuits, Different Cause for Delay

Timing parameters of digital circuits: Timing Parameters for Combinational Logic Gates, Timing Parameters for Sequential Circuits, Concept of Delay Path in a Design, Clock Concepts

Unit-II **08 hrs**

Resources for Static Timing Analysis Flow: Libraries, Netlist, Parasitics for Delay Calculation: Device Parasitics, Interconnects, Parasitics Extraction Formats, linear v/s. non-linear delay model. Wire load models, wire load modes, Delay calculations of different wire load models

Unit-III **07 hrs**

Concepts of Noise and Crosstalk for static timing Analysis: Coupling Capacitance Concept, Type of Crosstalk Noise or Glitch, Types of Crosstalk Delta Delay, Noise Libraries,

Crosstalk Effect on Timing Analysis, Strategy of Crosstalk on Nanometre Design: Cause for Crosstalk on Integrated Circuits, Crosstalk Prevention Methods.

Unit-IV **08 hrs**

Constraints for STA: Clock Constraints, Other Timing Constraints, 5.2.2 External Delays of DUA, Timing Exceptions: Multicycle Path, False Path, Clock Grouping, Case Analysis, Disable Timing, Path with Derate

Unit-V **08 hrs**

Timing Violations and Verification: Slack, Critical Path of Timing Report,Setup Violation, Hold Violation, Multicycle Path, Half Cycle Path, Timing Checks for Asynchronous Timing Paths, Recovery and Removal Violation Check, Input/Output Timing Path Checks ,DRC Violation Check,Multi Speed Clock Domain, Crosstalk Checks, Techniques to Fix Timing Violation: Techniques to Fix Setup Violations, Techniques to Fix Hold Violations

Text Books:

1. "Static Timing Analysis for VLSI circuits", R.Jayagowri, Pushpendra S. Yadav, MEDTECH, A Division of Scientific International , 2020.

Reference Book:

1. "Static Timing Analysis for Nanometer Designs: A Practical Approach", J. Bhasker, R. Chadha, Springer, 2009.

MOOC/ NPTEL courses:

- https://nptel.ac.in/courses/106/102/106102181/ NOC: synthesis of digital systems.

Course Title	**LOW POWER VLSI DESIGN**				
Course Code	**20ECVEPELP**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisites:

Course on Fundamentals of VLSI includes,
MOSFET characteristics, Implementation of different CMOS style circuits

Course outcomes:

At the end of the course, the student will have the ability to:

CO	**Course Outcomes**	**PO**
CO1	Extend the knowledge on basics of MOSFETs and Power Dissipation in MOS circuits to obtain the concepts of different techniques for power optimization.	PO3

CO2	Use the EDA tool to implement the designed circuit with techniques of power optimization in the design and justify obtained report by class room presentation.	PO2,3
CO3	Understand the journal research papers related to low power and updates their knowledge for new techniques to incorporate in projects of the specified stream.	PO1,3

Unit-I **08 hrs**

Sources of Power dissipation: Dynamic Power Dissipation -Short Circuit Power, Switching Power, Glitching Power, Static Power Dissipation, Degrees of Freedom.

Unit-II **08 hrs**

Supply Voltage Scaling Approaches: Device feature size scaling Multi-Vdd Circuits Architectural level approaches: Parallelism, Pipelining Voltage scaling using high-level transformations Dynamic voltage scaling Power Management.

Unit-III **08 hrs**

Switched Capacitance Minimization Approaches: Hardware Software Tradeoff Bus Encoding Two's complements Vs Sign Magnitude Architectural optimization Clock Gating Logic styles.

Unit-IV **08 hrs**

Leakage Power minimization Approaches: Variable-threshold-voltage CMOS (VTCMOS) approach Multi-threshold-voltage CMOS (MTCMOS) approach Power gating Transistor stacking Dual-V_t assignment approach (DTCMOS).

Unit-V **7 hrs**

Special Topics: Adiabatic Switching Circuits Battery-aware Synthesis Variation tolerant design CAD tools for low power synthesis

Text Books:

1. Pal, Ajit, Low-Power VLSI Circuits and Systems, Springer publisher, 2015

Reference Books:

1. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995.
2. Kaushik Roy and Sharat C. Prasad, Low-Power CMOS VLSI Design, Wiley-Inter science, 2000.

MOOC/Online courses:

- NPTEL http://nptel.iitm.ac.in Computer Science and Engineering, Department of Computer Science and Engineering ,IIT Kharagpur

Course Title	ADVANCED COMPUTER ARCHITECTURE				
Course Code	20ECVEPECA	Credits	3	L-T-P	3:0:0
CIE	50 Marks(100% weightage)	SEE		100 Marks (50% weightage)	

CO	Course Outcomes	PO
CO1	Acquire knowledge on the basic concepts of computer design, identifying the performance parameters and quantitative principles	PO3
CO2	Recognize the instruction level parallelism and different methods used for scheduling and structuring the code	PO3
CO3	Analyse the performance and Identify the limitations of ILP for the efficiency of multi pipeline architecture.	PO3
	Recognize the performance improvements by implementing shared memory and cache coherence	PO3
CO4	Make a report of the selected topic and present the same	PO2

Unit- I **08 hrs**

Introduction and Review of Fundamentals of Computer Design: Introduction; Classes computers; Defining computer architecture; Trends in Technology; Trends in power in Integrated Circuits; Trends in cost; Dependability, Measuring, reporting and summarizing Performance; Quantitative Principles of computer design.

Pipelining, Instruction –Level Parallelism, Exploitation and Limits on ILP: Introduction to pipelining, ILP; Crosscutting issues, fallacies, and pitfalls with respect to pipelining; Basic concepts and challenges of ILP.

Unit- II **08 hrs**

Memory Hierarchy Design, Storage Systems: Review of basic concepts; Crosscutting issues in the design of memory hierarchies; Case study of AMD Opteron memory hierarchy; Fallacies and pitfalls in the design of memory hierarchies.

Unit- III **07 hrs**

Advanced topics in disk storage: Designing and evaluating an I/O system – The Internet archive cluster; Case study of NetAA FAS6000 filer; Fallacies and pitfalls Definition and examples of real faults and failures; I/O performance, reliability measures, and benchmarks**,** Queuing theory; crosscutting issues.

Unit- IV **08 hrs**

Hardware and Software for VLIW and EPIC Introduction: Exploiting Instruction-Level Parallelism Statically, Detecting and Enhancing Loop-Level Parallelism, Scheduling and Structuring Code for Parallelism.

Unit- V **08 hrs**

Large-Scale Multiprocessors and Scientific Applications Introduction, Inter processor Communication: The Critical Performance Issue, Characteristics of Scientific Applications, Synchronization: Scaling Up, Performance of Scientific Applications on Shared-Memory Multiprocessors, Performance Measurement of Parallel Processors with Scientific Applications.

Text Books:

1. John L. Hennessey and David A. Patterson, "**Computer Architecture – A quantitative approach",** Morgan Kaufmann / Elsevier, Fifth edition, 2012.
2. Richard Y. Kain, "**Advanced Computer Architecture a Systems Design Approach**", PHI, 2011

Course Title	**EMBEDDED COMPUTING AND NETWORKING**				
Course Code	**20ECVEPEEC**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

CO	**Course Outcomes**	**PO**
CO1	**Understand** different types of Embedded Applications. Analyse various development tools, WAN, LAN and PAN protocols. Customize Linux for different environment. Port OS to embedded board and to build Arm tool Chain	**PO3**
CO2	Make an effective presentation of the selected topic	PO2

Unit- I **07 hrs**

Types of embedded application: Super loop, Interrupt driven, priority, round robin, OS based.

Embedded Android Architecture: Android Mobile and Tablet**,** Android TV, Android Wearable, Android Auto, Glass. **WAN** : MPLS, HHTP, MQTT, Coapetc. **LAN**: TCP / IP, UDP, Socket Programming, **PAN**: Bluetooth, BLE, zigbee

Unit- II **08 hrs**

Introduction to Software Development Tools: GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

Unit- III **08 hrs**

Interfacing Unit: Sensor and actuator interface, data transfer and control, GPS, GSM Unit-interfacing with data processing and display, Open CV for machine vision, Audio signal processing.

Unit- IV **08 hrs**

Building an Embedded System: Creating the Root File system, Building the Linux Kernel, Building the Root File system, Running UML, Networking.

Unit- V **08 hrs**

Embedded ARM Devices: Building ARM tool chain, Installing an Operating System on ARM board, Using ARM board Serial Port, Remote Serial Port.

Text books:

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Embedded Operating System - Alan Holt, Chi-Yu Huang, Springer
5. Intel® 64 and IA-32 Architectures Software Developer Manuals

Reference books:

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens

Course Title	**DEVICE MODELLING AND PROCESSING TECHNOLOGY**				
Course Code	**20ECVEPEMP**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

CO	**Course Outcomes**	**PO**
CO1	**Comprehend** fundamentals of semiconductors, theoretical and practical aspects of electronics technology	**PO3**
CO2	Ability to submit a report on the SPICE models fabrication process	**PO2**

Unit- I **08 hrs**

Fundamentals: Semiconductor Physics, Principle of circuit simulation and its objectives.

Introduction to SPICE: AC, DC, Transient, Noise, Temperature extra analysis.

Junction Diodes: DC, Small signal, large signal, High frequency and noise models of diodes, Measurement of diode model-parameters.

Unit- II **08 hrs**

Modelling of BJT: DC, small signal, high frequency and noise models of bipolar junction transistors. Extraction of BJT model parameters.

Unit- III **07 hrs**

MOSFETs: DC, small signal, high frequency and noise models of MOSFETs, MOS Capacitors. MOS.

Unit- IV **08 hrs**

Models: Level-1 and level-2 large signal MOSFET models. Introduction to BSIM models. Extraction of MOSFET model parameters.

JFET, MESFETs & HBTs: Modelling of JFET & MESFET and extraction of parameters. Principles of hetro-junction devices, HBTs, HEMT.

Unit- V **08 hrs**

CMOS Processing Technology: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements.

Text Books

1. S.M.Kang&Y.Leblibici, CMOS Digital Integrated Circuits-Analysis & Design, TMH, 3rd Ed.

2. S.M. Sze, Physics of Semiconductor Devices, Wiley Pub.

3. Neil H E Weste, David Harris, Ayan Banerjee, CMOS VLSI Design 3rd edition, Pearson Education.

Reference Books

1. Sedra and Smith, SPICE.

2. H.M. Rashid, Introduction to PSPICE, PHI.

3. B.G. Streetman & S. Baneerjee, Solid State Electronic Devices, PHI.

4. R. Raghuram, Computer Simulation of Electronic Circuits, Wiley Eastern Ltd.

Course Title	ADVANCES IN VLSI STRUCTURE				
Course Code	20ECVEPEAV	Credits	3	L-T-P	3:0:0
CIE	50 Marks(100% weightage)	SEE		100 Marks (50% weightage)	

CO	Course Outcomes	PO
CO1	Ability to understand multiple-gate MOSFET's. Strained-Si technology, thin body MOSFET's and Emerging nano materials.	PO3
CO2	Analyze short channel effect to define new structures and requirement of new materials	PO3
CO3	Analyse thin body MOSFET structure and impacts of substrate and nano materials on the performance	PO3
CO4	Use modern tool to simulate different structure and observe the performance comparison and make an effective documentation	PO2

Unit- I **08 hrs**

Transistor and multiple-gate MOSFET development, history, review of MOSFET principles and performance metrics

Unit- II **08 hrs**

Issues in short-channel MOSFET electrostatics; scale length fundamentals for thin-body MOSFETs (FinFET, planar Fully-Depleted SOI MOSFET and Gate-All-Around MOSFET)

Unit- III **08 hrs**

Advantages of thin body MOSFET's electrostatics quantum mechanical effects; effective carrier mobility; high-field velocities. Parasite resistance; thin-body MOSFET's carrier transport MOSFET compact modelling and Technology CAD (TCAD)

Unit- IV **08 hrs**

Impacts of substrate; Fin shape tuning; Gate stack process, FinFET's source/drain process, Multiple-gate MOSFET's threshold voltage engineering. Multiple-gate MOSFET performance dependence on channel orientation and Strained-Si technology and its effectiveness on Multiple-gate MOSFETs high-mobility channel transistors (Group III-V)

Unit- V **07 hrs**

Emerging nano materials: Nanotubes, nanorods and other nano structures, MOSFET like structure of carbon nano tubes.

Text Books/Reference Books:

1. Research papers
2. **MOOC**: http://www.flexilearn.ie/course/Nanoelectronics/43

RESEARCH METHODOLOGY

COMPULSORY TO ALL BRANCHES

Course Title	**RESEARCH METHODOLOGY & IPR**				
Course Code	**20ALLPICRM**	**Credits**	**2**	**L-T-P**	**2:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

CO	**Course Outcomes**	**PO**
CO1	Ability to write and present a substantial technical report/document	PO2
CO2	Able to demonstrate a degree of mastery over the area of specialization	PO3

Unit- I **08 hrs**

Meaning and sources of research problem, , Objectives and Characteristics of research – Errors in selecting research problem, Research methods Vs Methodology - Types of research-Criteria of good research – Developing a research plan.

Unit- II **08 hrs**

Investigations of a research problem - Selecting the problem - Necessity of defining the problem – Data collections-analysis- Importance of literature review in defining a problem - Survey of literature -Necessary instrumentations

Unit- III **08 hrs**

How to write paper-conference articles-poster preparation, thesis report writing, inclusion of references, journal reviewing process, journal selection process, filling about journal template, developing effective research proposal-plagiarism-research ethics

Unit- IV **08 hrs**

Nature of Intellectual property, IPRs- Invention and Creativity - Importance and Protection of Intellectual Property Rights (IPRs) – procedure for grant of patents and patenting under PCT-types of patents-technological research and innovation- international cooperation on IP.

Unit- V **7 hrs**

A brief summary of : Patents-Copyrights-Trademarks, patent rights-licensing and transfer of technology-patent databases-case studies on IPR-Geographical indications-new developments in IPR-protection of IPR rights

REFERENCE BOOKS:

1. Garg, B.L., Karadia, R., Agarwal, F. and Agarwal, U.K., 2002. An introduction to Research Methodology, RBSA Publishers.
2. Kothari, C.R., 1990. Research Methodology: Methods and Techniques. New Age International. 420p.
3. Anderson, T. W., An Introduction to Multivariate Statistical Analysis, Wiley Eastern Pvt., Ltd., New Delhi
4. Sinha, S.C. and Dhiman, A.K., 2002. Research Methodology, EssEss Publications. 2
5. Subbarau NR-Handbook of Intellectual property law and practise- S Viswanathan Printers and Publishing Private Limited 1998.

II SEMESTER

Program Core Course Syllabus

Course Title	**MIXED SIGNAL CIRCUIT DESIGN**				
Course Code	**20ECVEPCMS**	**Credits**	**4**	**L-T-P**	**3:0:1**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisite:

Analog IC design, Network theory

Course outcomes:

At the end of the course, the student will have the ability to:

CO	Course Outcomes	PO
CO1	Demonstrate, Design and build circuits for Data conversion in a mixed signal block	**PO3**
CO2	Demonstrate, Design and build circuits for clock generation and frequency synthesis	**PO3**
CO3	Submit a technical report of given mixed signal building blocks adding novelty to the existing solution	**PO1,2**

Unit-I **05 hrs**

Feedback amplifier: Types, topologies, Effect of Feedback on noise,

Unit-II **08hrs**

Oscillators, VCO: General consideration, Ring oscillator, LC oscillator, Voltage Controlled oscillator.

Unit-III **10 hrs**

PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

Unit-IV **08 hrs**

Switched capacitor circuits, Sampling switches, Switched capacitor Amplifiers.

Unit-V **08 hrs**

Data converter fundamentals,
Study of Data converters

Text Books:

1. Design of Analog CMOS Integrated Circuits, BehzadRazavi, TMH, 2007.

2. CMOS: Mixed Signal Circuit Design.–R. Jacob baker.

Reference Books:

1. Analog Integrated Circuit Design by Tony Chan Carusone, David A. Johns, Kenneth W. Martin.
2. CMOS Analog Circuit Design by Phillip Allen and Douglas R. Holberg.

MOOCS:

1. https://www.youtube.com/watch?v=XNWY857rdQo&t=1927s

Department of Electronics & Communication Engineering

LABORATORY EXPERIMENT LIST

Sl.No	Title of the Experiments
1.	**Design and Analyse** frequency response (Phase Margin, gain Margin) and noise for the following circuits for a given specification, a) Two Stage Operational amplifier, b) Folded Cascode Operational amplifier, c) Telescopic operational amplifier
2.	**Design** sub blocks of PLL and measure all the parameters.
3.	**Design** a simple ADC/DAC and analyse

Course Title	**DESIGN FOR TESTABILITY**				
Course Code	**20ECVEPCDT**	**Credits**	**4**	**L-T-P**	**3:1:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisites:

Basic courses on Digital circuit design, Simulation

Course outcomes:

At the end of the course, the student will have the ability to:

CO	Course Outcomes	PO
CO1	Apply the concept of faults and failure models to generate the number of fault models & Automatic Test Pattern Generator (ATPG) for the given design under test (DUT). Analyze and identify the given fault in given DUT(can be logic circuit or memory) and conclude the suitable available solution to test these faults. Ability to generate the Automatic Test Pattern Generation (ATPG) with different techniques using EDA tool	PO3
CO2	Engage on Literature survey and make an effort to suggest new solution as a team	PO1,2

Unit--I **05 hrs**

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

Unit--II **08 hrs**

Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG. Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits.

Unit--III **08 hrs**

Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

Unit--IV **08 hrs**

Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

Unit--V **10 hrs**

Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Power issues in IC Testing

Tutorials: **13 hrs**

Text books:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L.Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

Reference books:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, JaicoPublishing House.

2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

MOOC/NPTEL courses:

1. https://nptel.ac.in/courses/106/103/106103116/ : Design verification and test of digital circuits.

2. http://www.satishkashyap.com/2012/02/video-lectures-on-digital-hardware.htmlVideo , **Lectures** on Digital Hardware Design by Prof. M. Balakrishnan
3. https://nptel.ac.in/courses/106/103/106103182/Embedded systems: Design verification and Test.

Course Title	**Real Time Operating Systems**				
Course Code	**20ECVEGCRT**	**Credits**	**4**	**L-T-P**	**3:0:1**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisites:

Software aspects of embedded systems

Course outcomes:

At the end of the course, the student will have the ability to:

CO	Course Outcomes	PO
CO1	Design high performance software applications with real time deterministic response.	PO3
CO2	Configure and Optimize Embedded RTOS to achieve desired Performance and response.	PO3
CO3	Understand embedded system software stack. Realize RT applications using kernel services.	PO3
CO4	Make an effective oral presentation pertaining to RTOS and related high performance computing concepts.	PO2

Unit-I **10 hrs**

Basic concepts of RTOS: Defining RTOS, characteristics of RTOS, objects and services, Library-Based RTOS (Kernel-less approach), monolithic kernels, microkernels, virtual machines, Dockers and containers, embedded system software stack, kernel services.

Real time scheduling approaches: Clock driven, Static and dynamic scheduling, Fixed priority scheduling, preemptive Vs non preemptive methods in RT applications, EDF and RM techniques, feasibility check, writing schedulers, scheduling with any online scheduler.

Unit-II **10 hrs**

Priority related problems and solution: Critical Sections and Resource Management, Bounded and unbounded priority inversion**,** Deadlocks. Priority inversion avoidance using: Priority Inheritance Protocol (PIP), Priority Ceil Protocol (PCP), Higher Locker Protocol (HLP).

Unit-III **08 Hrs**

Semaphores and mutexes: Example Real Time application to demonstrate need, types of semaphores/mutexex, typical operations.

Inter Process Communication (IPC): Queues: States, typical operations, Queues within an Interrupt Service Routine, realization of Queue data structure, optimizing the code for performance enhancement, using built-in queue functions and writing optimized code, Pipes: Pipe states, pipe control blocks, typical operations,, mailbox and its use.

Unit-IV **05 hrs**

RTOS services: TCP/IP communication, client server model, sockets and ports, exception handling, interrupt mechanism

Unit-V **07hrs**

Comparison of available RTOS, Selection criteria of an RTOS for an IoT application
Application implementation: Process of designing firmware, boot loader, device drivers, developing interface code for module developed for any hardware: C program-based application layer code and kernel level code to configure and access data in/out of any chosen hardware.

Text Books:

1. Real-Time Concepts for Embedded Systems by Qing Li and Carolyn Yao ISBN: 1578201241 CMP Books

2. Mastering embedded Linux programming by Chris Simmonds Publisher: Packt Publishing, 2017 ISBN: 9781787283282 **OR** Using the free RTOS Real Time Kernel by Richard Barry, http://www.FreeRTOS.org

Reference Books:

1. Embedded and real time operating systems by Wang, K.C., Springer 2017, ISBN-10 : 3319515160 and ISBN-13 : 9783319515168

EBooks:

Real-Time Concepts for Embedded Systems QingLi with Caroline Yao Published by CMP BooksISBN:1578201241

MOOCs/online courses

Real-Time Systems by Dr Rajib Mall, IIT Kharagpur. For more details on NPTEL http://nptel.iitm.ac.in

Development of Real Time Systems by EIT Digital, coursera

LABORATORY EXPERIMENT LIST

Sl.No	Title of the Experiments
	PART A
7.	Create periodic, aperiodic, sporadic tasks, vary the attributes and analyze the effect, assign priorities, modify priorities, schedule using EDF/RM/other algorithm in any online scheduler and analyze the results with respect to CPU utilization and turnaround time.
8.	Simulate a given set of tasks using single and multiple CPUs. Analyze the results with respect to CPU utilization and latency.
9.	Write your own optimized scheduler using python or C for a given application.
10.	Schedule a set of given tasks using your own optimized scheduler and analyze the CPU utilization. Suggest methods to improve performance
	PART B (using freeRTOS/CMSIS)
1.	Task creation, priority assignment, scheduling, deletion (Verify/design scheduling algorithms and check its efficiency)
2.	Resource management: Semaphores and mutexes, priority inversion
3.	Queue management
4.	Interrupt management
	PART C (using any compiler)
1.	Develop a Queue Control block using C/C++. Outline its use with a user program.

II Semester electives

Course Title	SYSTEM VERILOG AND VERIFICATION				
Course Code	20ECVEPESV	Credits	3	L-T-P	3:0:0
CIE	50 Marks(100% weightage)	SEE		100 Marks (50% weightage)	

Prerequisites: Introductory course on Verilog, Knowledge about Simulation

Course outcomes: At the end of the course, the student will have the ability to:

CO	Course Outcomes	PO
CO1	Define, Understand and Explain OOPs concepts and system Verilog data types, Apply system Verilog constructs to create verification environment, Analyze coverage driven verification for given design under test(DUT)	PO3
CO2	Able to conceptualize and obtain 100% code coverage and functional coverage by determining the set of input constraints and assertions in test benches and able to document the effort to obtain coverage	PO3,2

Unit--I **06 hrs**

Verification Concepts: Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan**.**

Unit--II **09 hrs**

System Verilog: System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.

Unit--III **08 hrs**

System Verilog: SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism.

Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.

Unit--IV **08 hrs**

System Verilog: Assertions, Introduction to Assertion based verification, Immediate and concurrent assertions.

Coverage driven verification: Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

Building Test bench: Layered test bench architecture.

Unit--V **08 hrs**

Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

Reference Books:

1. 1. Janick Bergeron, Writing Testbenches Using SystemVerilog
2. Chris Spear, SystemVerilog for Verification
3. Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale, Verification Methodology Manual for SystemVerilog

MOOC/Online courses

- http://verificationexcellence.in/online-courses/learn-to-build-ovm-uvm-testbenches-from-scratch/
- https://nptel.ac.in/courses/106/105/106105165/ Hardware modeling using verilog

Course Title	**PHYSICAL DESIGN**				
Course Code	**20ECVEPEPD**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisite:

Structure of CMOS, Knowledge of EDA tools

Course outcomes:

At the end of the course, the student will have the ability to:

CO	**Course Outcomes**	**PO**
CO-1	Demonstrate the basic design flow in VLSI physical design automation and the basic algorithms used for implementing the same	**PO3**

CO-2	Make an Effective Documentation of Physical Design Flow using industry level EDA tool.	**PO2**

Unit—I **08 hrs**

Physical design flow, Libraries and File Formats. Introduction to physical design automation, Physical Design flow, EDA tools, Input files, Libraries: Standard Cells, Transistor Sizing, Input-Output Pads, Library Characterization, Constraints based design, File formats:Library Exchange Format (LEF), DEF (Design Exchange Format), Liberty Timing File (LIB). **08hrs**

Unit—II **08 hrs**

Partitioning and floor planning. Partitioning Techniques, Classification of Partitioning Algorithms, Floor planning, Design Style Specific Issues, macro placement, Floor planning Algorithms.

Unit—III **08 hrs**

Placement: Design Style Specific Placement Problems, Goals of placement, and Sanity checks before placement. Classification of Placement algorithms, Simulation Based Placement Algorithms: Simulated Annealing, Force Directed Placement, Interconnection Topologies, Estimation of Wire length.

Unit—IV **08 hrs**

Clock Tree Synthesis and Timing Analysis. Sanity checks before CTS. Need and goals of CTS. CTS related Terminologies. Clock skew reduction techniques and Topologies. Clock buffering mechanism. Post CTS Optimization. Basic timing related quantities.

Unit-V **07 hrs**

Routing and signoff checks, Goals of Routing, Routing Prerequisites, Routing Constraints, Global Routing, Track Assignment, Detail Routing, Routing algorithms. Design Rule Check (DRC), Layout versus Schematic (LVS), commonly faced LVS issues, IR Drop Analysis: Static IR drop analysis, Dynamic IR drop analysis, Methods to reduce IR drop: ELECTRO MIGRATION (EM): Methods to fix EM

Text Book

1. KhosrowGolshan,“Physical Design Essentials-An ASIC Design Implementation Perspective”, 2007 Springer Science+Business, Media

2. Sherwani, Naveed A. "Algorithms for VLSI Physical Design Automation"

Reference books:

1. Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill International Edition 1995.
2. Preas M. Lorenzatti, " Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.
3. S H Gerez, " Algorithms for VLSI Design Automation", Wiley, India, 2nd edition

MOOCS:

1.https://www.youtube.com/watch?v=lRpt1fCHd8Y&list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk

2.https://www.youtube.com/watch?v=TDvq1hVXzRc&list=PLDYvivDnqWMMNIOh511ep2sr6nmlhMInY&index=2

Course Title	**HARDWARE-SOFTWARE CO-DESIGN**				
Course Code	**20ECVEPEHS**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

CO	**Course Outcomes**	**PO**
CO1	Understand fundamental issues in co-design, Learn about prototyping and emulation,.	PO3
	Understand compilation techniques, and learn related tools. Acquire ability to differentiate various target architectures	PO3
CO2	Acquire ability to generate specifications and develop verification plans and make a documentation.	PO2

Unit- I **08 hrs**

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

Unit- II **08 hrs**

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Unit- III **08 hrs**

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Unit- IV **08 hrs**

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Unit- V **07 hrs**

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

Text books:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.

2. Hardware / Software Co- Design - Giovanni De Micheli Maria Giovanna Sami, 2002, Kluwer Academic Publishers

Reference books: 1. A Practical Introduction to Hardware/Software Co-design - Patrick R. Schaumont - 2010 – Springer

Course Title	SYSTEM ON CHIP ARCHITECTURE				
Course Code	20ECVEPESC	Credits	3	L-T-P	3:0:0
CIE	50 Marks(100% weightage)	SEE		100 Marks (50% weightage)	

CO	Course Outcomes	PO
CO1	**Apply** concepts of Moore's law, CMOS scaling to understand the System on Chip with its need, evolution, challenges, goals, superiority over system on board & stacked ICs in package. **Analyze**Typical goals in SoC design and also inter connect architecture	**PO3**
CO2	**Design** solutions for issues at system level, and issues of Hardware-Software co design and make an effective presentation.	**PO2**

Unit- I **08 hrs**

Review of Moore's law and CMOS scaling, benefits of System On Chip integration in terms of cost, power, and performance. Comparison on System on Board, System on Chip, and System-in-Package. Typical goals in SoC design cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

Unit- II **08 hrs**

System On Chip Design Process: A canonical SoC Design, SoC Design flow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software co design, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc.

Unit- III **08 hrs**

Embedded Memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

Unit- IV **08 hrs**

Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in anNoC. Packet switching and wormhole routing.

Unit- V **07 hrs**

MPSoCs: What, Why, How MPSoCs, Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design

Case Study: A Low Power Open Multimedia Application Platform for 3G Wireless.

Reference Books:

1. SudeepPasricha and NikilDutt,**"On-Chip Communication Architectures: System on Chip Interconnect"**, Morgan Kaufmann
Publishers © 2008.
2. Rao R. Tummala, MadhavanSwaminathan, **"Introduction to system on package sop-Miniaturization of the Entire Syste"**,
McGraw-Hill, 2008.
3. James K. Peckol, **"Embedded Systems: A Contemporary Design Tool"**, Wiley Student Edition.
4. Michael Keating, Pierre Bricaud, **"Reuse Methodology Manual for System on Chip designs"**, Kluwer Accademic Publishers, 2nd
edition, 2008.
5. Sung-Mo Kang, Yusuf Leblebici, **"CMOS Digital Integrated Circuits"**, Tata Mcgraw-Hill, 3rdEdition.

Course Title	**MEMORY DESIGN AND TESTING**				
Course Code	**20ECVEPEMD**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

CO	**Course Outcomes**	**PO**
CO1	Acquire the knowledge on Semiconductor memories, Apply the knowledge of CMOS technology and electronic circuits theory to design semiconductor memories,Analyze different types of memories**,** Apply the knowledge of CMOS technology and electronic circuits theory to design semiconductor memories	**PO3**
CO2	Ability to submit a report on the impact/growth of Advanced Memory Technologies for societal and sustained development.	**PO2**

Unit- I **08 hrs**

Random Access Memory Technologies: SRAM Cell Structures-MOS SRAM Architecture, MOS SRAM Cell and Peripheral, Circuit Operation, Bipolar SRAM Technologies, Silicon On Insulator (SOl) Technology, Advanced SRAM Architectures and Technologies, Application Specific SRAMs.

Unit- II **08 hrs**

Dynamic Random Access Memories (DRAMs): DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs, Soft Error

Failures in DRAMs, Advanced DRAM Designs and Architecture, Application Specific DRAMs.

Unit- III **08 hrs**

Non-volatile Memories: Masked Read-Only Memories (ROMs), High Density ROMs, Programmable Read Only Memories (PROMs), Bipolar PROMs, CMOS PROMs, Erasable (UV), Programmable Road-Only Memories (EPROMs), Floating-Gate EPROM Cell, One-Time Programmable (OTP) EPROMS, Electrically Erasable PROMs (EEPROMs), EEPROM Technology and Architecture, Non-volatile SRAM, Flash Memories (EPROMs or EEPROM), Advanced Flash Memory Architecture.

Unit- IV **08 hrs**

Memory Fault Modelling, Testing and Memory Design For Testability and Fault Tolerance. RAM Fault Modelling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Non-volatile Memory Modelling and Testing, IDDQ Fault Modelling and Testing, Application Specific Memory Testing.

Unit- V **07 hrs**

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory Reliability, Reliability Modelling and Failure Rate Prediction. Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification. Radiation Effects, Single Event Phenomenon (SEP), Radiation Hardening Techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test Structures.

Text Books

1. A.K Sharma, “Semiconductor Memories Technology, Testing and Reliability”, IEEE Press.
2. Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill.
3. Belty Prince, “ Semiconductor Memory Design Handbook”
4. Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor.

Course Title	Digital System Design Using FPGAs				
Course Code	20ECVEPEDS	Credits	3	L-T-P	3:0:0
CIE	50 Marks(100% weightage)	SEE		100 Marks (50% weightage)	

Prerequisites:

Digital Electronic circuits and Fundamentals of Hardware Descriptive Languages
Course outcomes:

At the end of the course, the student will have the ability to:

CO	Course Outcomes	PO
CO1	Analyze the Programmable Logic Devices (CPLDs and FPGAs)	PO3
CO2	Develop and analyze a Digital System on FPGA fabric	PO3
CO3	Implement the Digital system effectively on the FPGA fabric using different approaches	PO3
CO4	Optimize the design performance for power, area and delay.	PO3

Unit-I **8 hrs**
Introduction to Programmable logics

Unit-II **10 hrs**
Programmable logic based FPAG architecture- General Fabric and Routing Resources Special Primitives, Block RAM (Memory) ,Clocking, Special I/O Features

Unit-III **10 hrs**
Processor system based FPGA architecture What Is a Processor Instruction Sets, Memory, Initial Design, The ALU, The Program Counter, Processor, Program and The Assembler

Unit-IV **05 hrs**
FPGA synthesis constraints, Advanced Timing and Clock Domains, Breaking Timing and Fixing It with Pipelining,

Unit-V **06 hrs**
Design Methodology by applying constrains: Selection of FPGA fabric, Selection of Boolean functions, Selection of Slice and LUT, Creating the hard macro of the design.

Reference Books:
1. Learning FPGAs -Digital Design for Beginners with Mojo and Lucid HDL 1st Edition By Justin Rajewski Published by O'Reilly Media, Inc., 1005 Gravenstein Highway North, Sebastopol, CA 95472.

2. Digital System Design with FPGA Implementation Using Verilog and VHDL
By Cem Unsalan, Bora Tar, McGraw-Hill Education, 2017 ISBN 1259837904, 9781259837906

Open elective

COURSE TITLE	**Introduction to Scripting Languages**				
COURSE CODE	**20ECVEGESL**	**Credits**	**4**	**L-T-P**	**4:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisites:

Fundamentals of command line interface in windows/Linux/Unix Environments,
Basic Programming skills.

Course Outcomes:
At the end of the course, the student will have the ability to:

CO	**Course Outcomes**	**PO**
CO1	Understand, Analyse and execute scripts for automation of tool commands in CAD tools	PO3
CO2	Create and execute scripts using Bash/Perl/TCL and automate CAD design flow and design verification flow on open source tools	PO3

Unit--I **05 hrs**
Overview of Scripting Languages – Bash, Tcl, PERL, CGI, VB Script, Java Script.

Unit-II **05 hrs**
Bash: List, Arrays and hashes

Unit-III **10 hrs**
Tcl: Basic Syntax Commands, Data types, Variables, Operators, Decisions, Loops, Arrays, Strings, Lists, Procedures and Packages

Unit-IV **10 hrs**
PERL: Variables, data types, Operators, Scalars, hashes, loops, subroutines, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

Unit-V **10 hrs**

Introduction to open source CAD tools and applications of scripting in CAD applications; Case study with Icarus Verilog and Verilator

Text Books:

1. Bash Guide for Beginners by MachteltGarrels,
2. Fundamentals of tcl by brent welch and Scripting with Perl and Tcl by Hans Petter Langtangen

Reference Books:

1. http://heim.ifi.uio.no/~inf3330/perl.pdf
2. Bash Reference Manual :https://www.gnu.org/software/bash/manual/bash.html

III SEMESTER

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Elective 5

Course Title	**Advanced FPGA Design**				
Course Code	**20ECVEGEAF**	**Credits**	**3**	**L-T-P**	**2:1:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisites:

In-depth understanding of Digital Electronic circuits and Fundamentals of Hardware Descriptive Languages

Course outcomes:

At the end of the course, the student will have the ability to:

CO1	Analyze the System for its feasibility on the reconfigurable FPGA hardware	PO3
CO2	Develop the system for an efficient utilization of FPGA resources	PO3
CO3	Implement the System effectively on FPGAs by understanding the basic machine learning algorithms	PO3
CO4	Optimize the design performance for power, area and delay by applying the ML algorithms.	PO3

Unit-I: Design factors for FPGA (Speed and Power) **04** hrs.
Clock Control, Input Control, Reducing the Voltage Supply, Dual-Edge Triggered Flip-Flops

Unit-II: Design factors for FPGA (Area**)** **04hrs**
Rolling Up the Pipeline, Control-Based Logic Reuse, Resource Sharing, Impact of Reset on Area

Unit-III: RESET Circuits **06 hrs.**
Asynchronous Versus Synchronous, Mixing Reset Types, Multiple Clock Domains

Unit-IV: High Level Design **05hrs**
Abstract Design Techniques, Graphical State Machines, DSP Design

Unit-V: Example Design **07 hrs.**
AES Architectures, Performance Versus Area, Other Optimizations: Machine learning for FPGA implementations

Reference Books:

1. Advanced FPGA Design: Architecture, Implementation, and Optimization by Steve Kilts ISBN: 978-0-470-05437-6 June 2007 Wiley-IEEE Press

2. Digital System Design with FPGA Implementation Using Verilog and VHDL By Cem Unsalan, Bora Tar ,McGraw-Hill Education, 2017 ISBN 1259837904, 9781259837906

Course Title	**UVM METHODOLOGY CONCEPTS**				
Course Code	**20ECVEGEUV/20ECVEGEUV**	**Credits**	**3**	**L-T-P**	**2:1:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisite:

HDL Programming and System Verilog verification methodologies

Course outcomes:

At the end of the course, the student will have the ability to:

CO1	Perform verification using Universal Verification Methodology	PO3
CO2	Develop Reusable Open Verification Components	PO3

Unit-I **08 hrs**

Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

Unit-II **08 hrs**

Over view of OVM Environment with OVM Libraries, Introduction toOVM, OVM and Coverage-Driven Verification (CDV), Test bench and Environments. OVC Overview. Data Item (Transaction). Driver (BFM). Sequencer. Monitor. Agent. Environment. The System Verilog OVM Class Library. OVM Facilities.

Unit-III **08 hrs**

Transaction-Level Modeling (TLM). Transaction-Level Modeling Overview. TLM Basics. Transaction-Level Communication. Basic TLM Communication. Communicating Between Processes. Blocking versus Nonblocking. Connecting Transaction-Level Components. Peer-to-Peer connections. Port/Export Compatibility. Encapsulation and Hierarchy. Hierarchical Connections. Analysis Communication, Ports, Exports.

Unit-IV **08 hrs**

Developing Reusable Open Verification Components (OVCs)

Modelling Data Items for Generation. Inheritance and Constraint Layering. Defining Control Fields ("Knobs"). Transaction-Level Components. Creating the Driver. Creating the Sequencer. Connecting the Driver and Sequencer. Fetching Consecutive Randomized Items. Sending Processed Data Back to the Sequencer.

Unit-V **07 hrs**

Using TLM-Based Drivers. Creating the Monitor. Instantiating Components. Creating the Agent. Creating the Environment. The Environment Class. The OVM Configuration Mechanism.

References

OVM User Guide, Version 2.1.2, © 2008–2011 Cadence Design Systems, Inc. (Cadence). All rights reserved. Cadence Design Systems, Inc., 2655 Seely Ave., San Jose, CA 95134, USA. © 2008–2011 Mentor Graphics, Corp. (Mentor). All rights reserved. Mentor Graphics, Corp., 8005 SW Boeckman Rd., Wilsonville, OR 97070, USA
http://www.specman-verification.com/source_bank/ovm-2.1.2/ovm-2.1.2/OVM_UserGuide.pdf

Verification Methodology Manual for System Verilog, © 2008–2011 Cadence Design Systems, Inc. (Cadence). All rights reserved. Cadence Design Systems, Inc., 2655 Seely Ave., San Jose, CA 95134, USA. © 2008–2011 Mentor Graphics, Corp. (Mentor). All rights reserved.
Mentor Graphics, Corp., 8005 SW Boeckman Rd., Wilsonville, OR 97070, USA
http://read.pudn.com/downloads178/ebook/825398/vmm_sv.p

Course Title	**Machine Learning and AI**				
Course Code	**20ECVEGEML/20ECELGEML**	**Credits**	**3**	**L-T-P**	**3:0:0**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

Prerequisites: Programming in C/ C++ and Python

Course outcomes:
At the end of the course, the student will have the ability

CO1	To infer on the dynamics, design and performance of ML paradigms using relevant mathematical paradigms	PO3
CO2	To condition, portray and model engineering systems for a gamut of ML based techniques	PO3
CO3	To analyse the performance of ML techniques vis-à-vis conventional techniques in a quantitative manner	PO3

Unit-I **09hrs**
Linear Models for Classification: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Models, The Laplace Approximation, Bayesian Logistic Regression, Exercises

Unit-II **06hrs**
Neural Networks: Feed-forward Network Functions, Network Training, Error Back propagation, The Hessian Matrix, Regularization in Neural Networks, Mixture Density Networks, Kernel Methods, Radial Basis Function Networks, Gaussian Processes, Exercises

Unit-III **06 hrs**
Sparse Kernel Machines: Maximum Margin Classifiers, SVMs for regression, Relevance Vector Machines, RVM for regression, RVM for classification, Exercises

Unit-IV **06hrs**
Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Linear-Gaussian models, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Mixture Models: K-means Clustering, Mixtures of Gaussians, An Alternative View of EM, The EM Algorithm in General, Exercises

Unit-V **09hrs**
Approximate Inference: Variational Inference, Illustration: Variational Mixture of Gaussians, Variational distribution, Predictive density, Induced factorizations, Variational Linear Regression, Variational distribution, Predictive distribution, Local Variational Methods,

Optimizing the variational parameters, Inference of hyperparameters, Expectation Propagation, Exercises

Text books:

1. Pattern Recognition and Machine Learning, Christopher M. Bishop
2. Machine Learning: A Probabilistic Perspective (Adaptive Computation and Machine Learning series) 1st Edition, Kevin P. Murphy

REFERENCE BOOKS:

1. Artificial Intelligence: A Modern Approach, Stuart J. Russell and Peter Norvig
2. Deep Learning, Ian Goodfellow, Yoshua Bengio, and Aaron Courville
3. Machine Learning, Tom M. Mitchell
4. Fundamentals of Machine Learning for Predictive Data Analytics: Algorithms, Worked Examples, and Case Studies (The MIT Press) 1st Edition, by John D. Kelleher, Brian Mac Namee, Aoife D'Arcy
5. Machine Learning: A Bayesian and Optimization Perspective (Net Developers) 1st Edition, Sergios Theodoridis

Course Title	**PROJECT WORK(PHASE-1)**				
Course Code	**20ECVEPWP1**	**Credits**	**8**	**L-T-P**	**0:0:8**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

	Course Outcomes of phase-1	
CO1	Identify a suitable project by making use of the technical and engineering knowledge gained from previous courses with the awareness of impact of technology on the Society and their ethical responsibilities.	PO3
CO2	Collect and disseminate information related to the selected project within given time frame.	PO1
CO3	Communicate technical and general information by means of oral as well as written Presentation skills with professionalism.	PO2

Course Title	INTERNSHIP				
Course Code	**20ECVEPCIN**	**Credits**	**9**	**L-T-P**	**0:0:9**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

	Course Outcomes of Internship	
CO1	Ability to develop a sound theoretical and practical knowledge of new technologies.	PO3
CO2	Ability to Develop domain specific problem solving and critical thinking skills, individual responsibility towards their internship goal as well as participate as an effective team member, to gain exposure to professional work culture & practices	PO3
CO3	Develop effective presentation & communication skills, and create proper documentation of the work	PO2

Course Title	TECHNICAL SEMINAR-1				
Course Code	**20ECVESR01**	**Credits**	**2**	**L-T-P**	**0:0:2**
CIE	**50 Marks(100% weightage)**	**SEE**		**100 Marks (50% weightage)**	

CO1	Identify the problem through literature survey by applying depth knowledge of the chosen domain	PO1,3
CO2	Analyse, synthesize and conceptualize the identified problem	PO3
CO3	Communicate clearly, write effective reports and make effective presentations following the professional code of conduct and ethics	PO2
CO4	Comprehensively study the domains and reflect the same towards the future enhancements of the work	PO2

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Course Title	TECHNICAL SEMINAR-2				
Course Code	20ECVESR02	Credits	2	L-T-P	0:0:2
CIE	50 Marks(100% weightage)	SEE		100 Marks (50% weightage)	

COURSE OUTCOMES

CO1	Identify the problem through literature survey by applying depth knowledge of the chosen domain	PO1,3
CO2	Analyse, synthesize and conceptualize the identified problem	PO3
CO3	Communicate clearly, write effective reports and make effective presentations following the professional code of conduct and ethics	PO2
CO4	Comprehensively study the domains and reflect the same towards the future enhancements of the work	PO2

Course Title	PROJECT WORK (PHASE-2)				
Course Code	20ECVEPWP2	Credits	20	L-T-P	0:0:20
CIE	50 Marks(100% weightage)	SEE		100 Marks (50% weightage)	

	COURSE OUTCOMES(Phase-2)	
CO1	Identify the modern tools required for the implementation of the project.	PO3
CO2	Design, examine critically and implement or develop a prototype for the identified problem during phase I	PO1
CO3	Communicate technical information by means of oral as well as written presentation skills with professionalism.	PO2